DSG-NPS R&D Meeting

Date: September 15, 2020 **Time:** 11:00 – 12:00

<u>Attendees</u>: Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, George Jacobs, Tyler Lemon, Marc McMullen, Amrit Yegneswaran

- 1. CSS screen development status
 - 1.1. EPICS screens created by Mary Ann will be moved to a computer on the Hall B subnet for testing
 - 1.2. Voltage and current limit settings screens for each PMT—108 of 1080 screens completed
- 2. CAEN testing and data analysis
 - 2.1. George will be completing all testing data analysis using Excel; eight modules remain to be analyzed for voltage stability
 - 2.2. Decided on ~740 μ A as the trip threshold and 1 s for time over threshold for the trip test being developed
 - 2.3. Brad dropped off four A1535 modules for testing/troubleshooting; contacting CAEN for firmware
- 3. An Omega 4-wire RTD (PT100) is the front runner for temperature sensors to be used in hardware interlock system
- 4. HV divider cables fabricated—760 of 1100
- 5. Voltage rating issues still awaiting decision